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computer science 12

# Bachelor/Master Thesis

## Non-Volatile Memory Aware Task Scheduling on Low Power Hardware

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The commercial availability of non-volatile memory (NVM) as byte-addressable random-access memory (RAM) yields new design principles in the system software and the application level. FRAM [1] is a prominent example of a low power NVM, which can be found as on-chip RAM on some microcontrollers. The MSP430FRxxx series from Texas Instruments (TI) provides low cost mikrocontrollers, which are publicly available. These microcontrollers employ an on-chip FRAM in addition to on-chip SRAM. Thus, a hybrid memory architecture with volatile memory (VM) and non-volatile memory is provided.


Figure 1: TI MSP430 FR6989 with 128kb of FRAM

Both, the volatile and the non-volatile memory are addressable at distinct address regions in the CPU address space. Therefore, software can actively decide if memory contents are stored in VM or NVM. However, this decision should not be made by the individual application, indeed the operating system should provide an abstraction to properly store and migrate applications on VM and NVM.
When it comes to task scheduling, task memory may be distributed between VM and NVM. The `text` segment, for instance, may be stored in the NVM, while the `stack` may be desired to be stored in the VM. When the system enters a lowe-power mode, the VM can be turned off to reduce the energy consumption further. Thus, after waking up from the low-power mode, all contents in the VM are deleted. Task scheduling, as a specific instance, has to be aware of this and migrate the volatile part of the task's memory to the NVM, before entering the low-power mode.

**In this thesis**, students should get familiar with the provided hardware platform (TI MSP430FR6989). Students should study the CPU execution model, interrupt routines and specifics of the low-power modes. Students should understand what happens when the device enters the low-power mode and what actions are required. Subsequently, studenty should extend a simple task scheduler, to let it place task's memory in the VM and backup this memory to the NVM before entering the low-power mode. The backup has to be restored after waking up the system again, such that the task execution can continue without errors. The implementation should further offer the freedom of choice to a task, which memory content's are stored in the VM and NVM. On a `heap` memory allocation, for instance, the tas may choose if the memory is allocated to NVM or VM.

*Other suggestions and related topics are also welcome. Please do not hesitate to make an appointment.*

**Required Skills:**

- Knowledgeable of C and C++ programming
- Willing to program microcontrollers
- Basic knowledge about operating systems and scheduling

**Acquired Skills after the thesis:**

- Knowledge about modern memory technologies and memory access latency models.
- Knowledge about MSP430 microcontrollers and the integrated FRAM memory.
- Detailed knowledge about scheduler implementations

[1] Choi, Ja Moon. "Ferroelectric RAM device." U.S. Patent No. 6,044,008. 28 Mar. 2000.