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Bachelor/Master Thesis

Precise Access Latency Measurement for Integrated FRAM Devices

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Byte-addressable non-volatile memories (NVMs) recently have emerged to serve as main memory due to the features of low leakage power, high density, and low unit costs. However, only a few NVM technologies are mature and publicly available at the moment. The limited availability of NVMs leads to theoretical models not being validated on real hardware in most cases. Since Ferroelectric RAM (FRAM) [1] is a mature technology and is publicly available on the market, it is actually possible to verify theoretical models on a real device.

Figure 1: TI MSP430 FR6989 with 128kb of FRAM

The access latency of a memory device is typically influenced by two major factors: 1) The access latency of a single memory cell determines the required time to read a single bit (or multiple bits in case of Multi Level Cells (MLC)). 2) The assembly of memory cells to a final memory chip determines the latency between a memory request and the sensing of the actual cell. While the single cell access latency may be maintained as a constant by the memory controller, the memory layout specific latency can vary for each memory access, due to different row buffer contents. However, considering this theory leads to a theoretic access latency model, which still needs to be enriched with concrete numbers.

One way to measure access latencies is to record the consumed time for a big number of memory accesses with the help of a timer. This usually leads to imprecise results due to side effects. As an alternative, the maximum wait time for a memory content can be configured on the TI MSP430 FR6989 microcontroller. By recording the memory access fail rate for a fixed wait time, also a statistical distribution of access latencies can be derived. This method cannot be influenced by side effects of the CPU, since the timing limitation is implemented in the memory controller.

In this thesis, students first should get familiar with the MSP430 microcontroller family, especially with the MSP430 FR6989 model. After being able to run simple programs on the real hardware, students should study the device specific datasheet and interact with the FRAM controller. The controller should be programmed with a fixed wait time and exceptions of a failed memory access should be caught. Finally, the measured access latency should be used to enrich a simple theoretical model with real numbers. Students should note that, the involved source code this thesis will be publicly released and should be fully documented to comply the rationale of open-source software development.

Other suggestions and related topics are also welcome. Please do not hesitate to make an appointment.

Required Skills:

- Knowledgeable of C and C++ programming
- Willing to program microcontrollers

Acquired Skills after the thesis:

- Knowledge about modern memory technologies and memory access latency models.
- Knowledge about MSP430 microcontrollers and the integrated FRAM memory.

[1] Choi, Ja Moon. "Ferroelectric RAM device." U.S. Patent No. 6,044,008. 28 Mar. 2000.