Robust and Efficient Machine Learning for Emerging Resource-Constrained Embedded Systems

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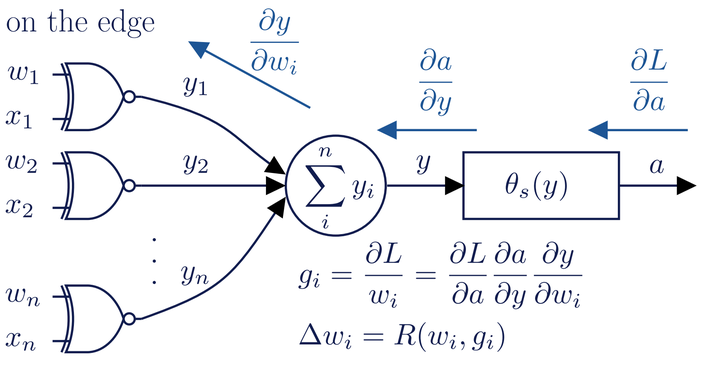
Vision of this Thesis

Robust BNNs with approximate memory and computing units, while training on the edge

- BNN robustness optimization
- HW/SW codesign methods for robust and efficient BNN inference
- Train BNNs efficiently on the edge

w_i	x_i	y_i
0	0	1
0	1	0
1	0	0
1	1	1

$w_i, x_i, y_i, a \in \{0,1\}$
$s, y \in \mathbb{Z}$
$\theta_s(y) = \begin{cases} 1 & y > s \\ 0 & else \end{cases}$



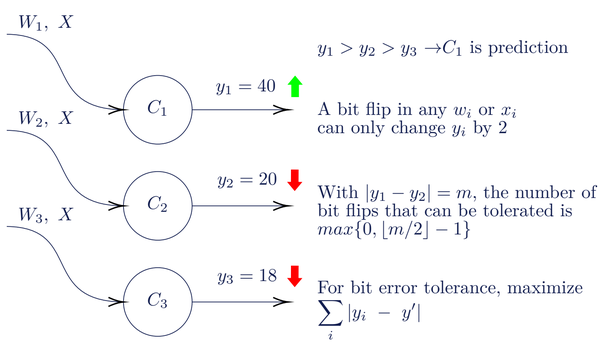
$g_i = \frac{\partial L}{w_i} = \frac{\partial L}{\partial a}\frac{\partial a}{\partial y}\frac{\partial y}{\partial w_i}$

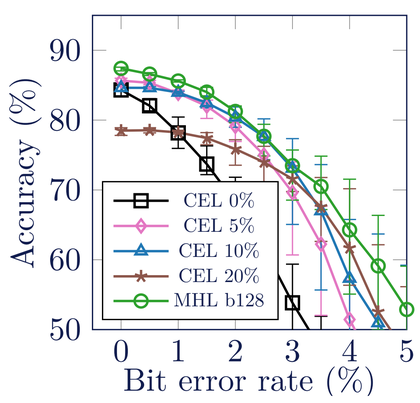
$\Delta w_i = R(w_i, g_i)$

Robustness Optimization of BNNs

Goal: Achieve robustness without bit flip injection

- Classes: C_i. Index i of neuron with largest output determines predicted class index
- MHL maximizes the margins between the outputs of the last-layer neuron
- Margin-maximization leads to robustness without the need of error models

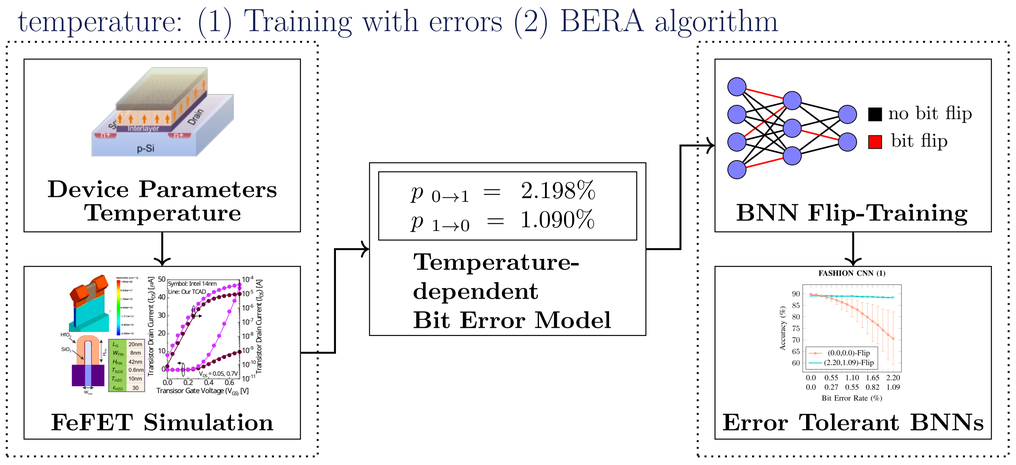




BNNs with FeFET Memory

Explore FeFET memory as on-chip memory for BNNs

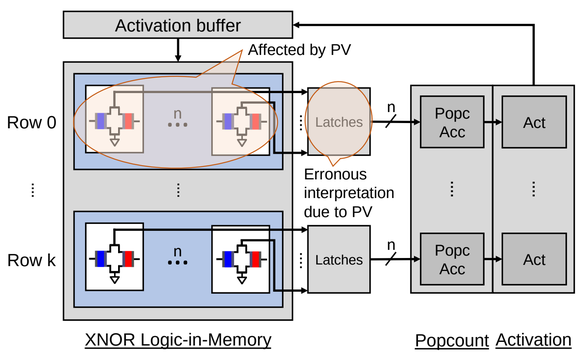
- FeFET sensitive to temperature fluctuations, unacceptable BNN accuracy drop
- Countermeaures achieve temperature tolerance across entire range of operating temperature: (1) Training with errors (2) BERA algorithm

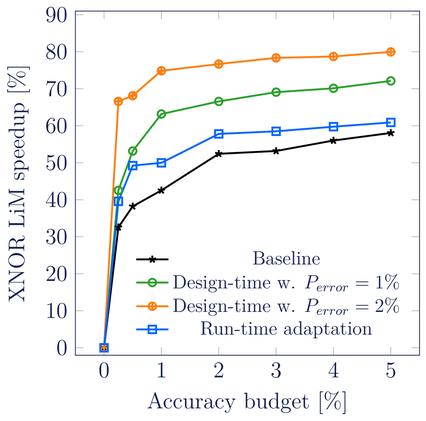


BNNs with FeFET-based XNOR LiM

Trade off speed of FeFET-based XNOR gates with BNN reliability

- BNNs employ approximate FeFET-based XNOR gates for LiM
- Investigate the probability of error in FeFET-based XNOR LiM
- Exploit robustness of BNNs, trading off speed and reliability using the design objective $WSAD_{\ell,p_\ell} = \frac{s_{\ell,p_\ell}}{AD_{\ell,p_\ell}} \frac{c_\ell}{c_{max}}$

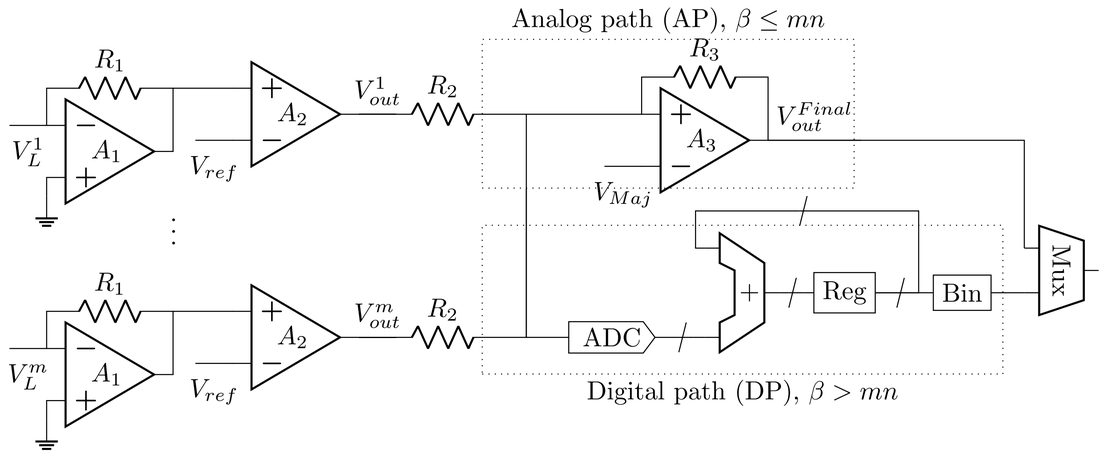




Efficient Analog-based BNN Accelerators

Analog BNN accelerators use lots of ADCs → Expensive designs!

- LTA approximates global thesholdings by local thresholdings
- Using LTA, ADCs and digital components are not required or only used rarely
- Area and energy usage significantly smaller in LTA circuit compared to SOTA

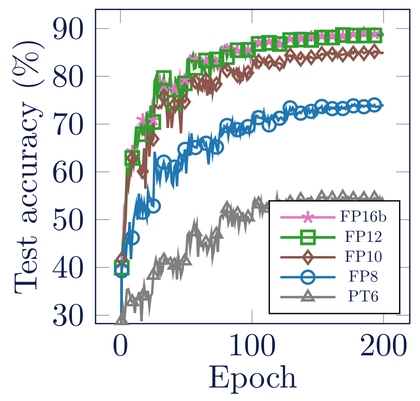


Efficient BNN Training on the Edge

Efficient BNN training through reduced FP formats

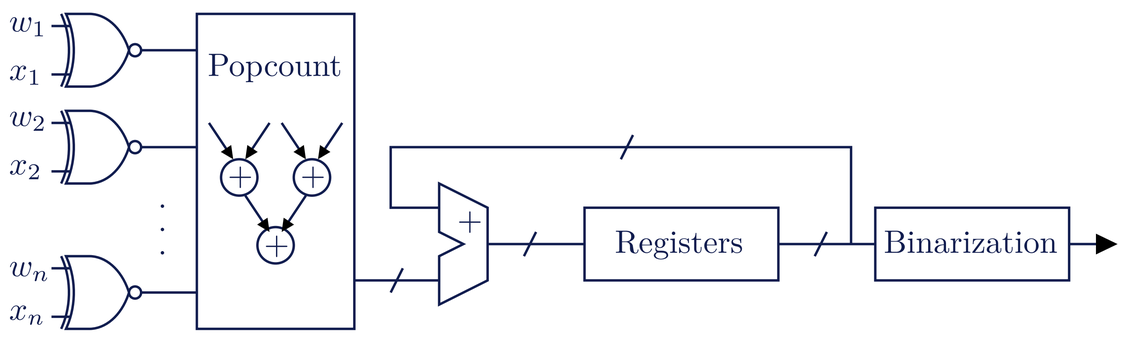
- Bias: $b = -\lfloor \log_2(m_{sample}^{absmax}) \rfloor + 1$
- Exponent: $c = \lceil \log_2(-\log_2(\alpha\tau) - b + 1) \rceil$
- Mantissa: $U(Q, \mathbf{M}_t) = \frac{1}{|\mathbf{M}_t|} \sum_{m_t \in \mathbf{M}_t} \mathbf{1}\left[|\Delta m_t| < \frac{|Q(m_t) - q_{v^*}|}{2}\right]$

Encoding	Range	Precision	Realization
PT6	o	-	1 sign, 5 exp.
FP8	o	o-	1 sign, 5 exp., 2 mant.
FP10	o	o-	1 sign, 5 exp., 4 mant.
FP12	o	o	1 sign, 5 exp., 6 mant.
FP16b	+	o	1 sign, 8 exp., 7 mant.
FP32	+	+	1 sign, 8 exp., 23 mant.



Research tools available: github.com/myay

- SPICE-TORCH: Connect SPICE and PyTorch simulations
- TREAM: Error evaluations of tree-based models in sklearn
- DAEBI: Enables design space exploration of BNN accelerators in VHDL regarding different accelerator architectures and dataflows



Acknowledgements

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